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Recent Results on SEU Hardening of SiGe HBT Logic Circuits

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Outline

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- **Introduction**
- **TID and SEU in SiGe Technology**
- **RHBD Techniques**
  - Circuit-Level Techniques
  - Device-Level Techniques
- **Experiment**
- **Heavy-Ion Data and Analysis**
- **Summary**

Introduction

- **SiGe HBT technology is robust to TID radiation, as built**
- **However, TID tolerance does not ensure SEU tolerance**

Objectives:

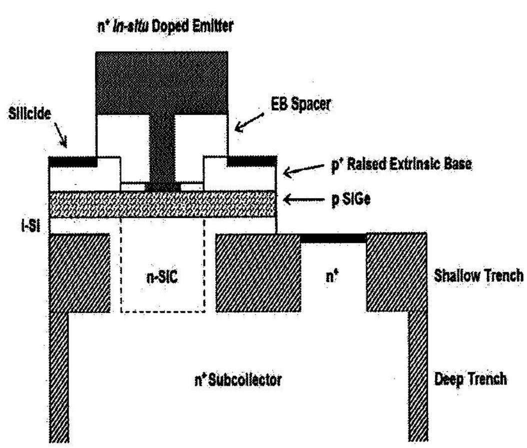
- **Develop RHBD techniques for SiGe technology**
  - identify candidate device and circuit-level RHBD approaches
- **Implement digital building blocks in IBM SiGe 8HP**
- **Experimentally evaluate effectiveness of RHBD approaches**

End Goal:

"Total Dose and SEU Tolerant SiGe HBT Devices / Circuits"

SiGe Technology

- **3rd-Generation SiGe HBT Technology (200 GHz) – IBM 8HP**
  - **0.12 um emitter width**
  - **raised extrinsic base**
  - **reduced thermal cycle**
  - **in-situ polysilicon emitter**
  - **deep trench isolation**
  - **shallow trench isolation**
  - no radiation hardening!



Proton Response

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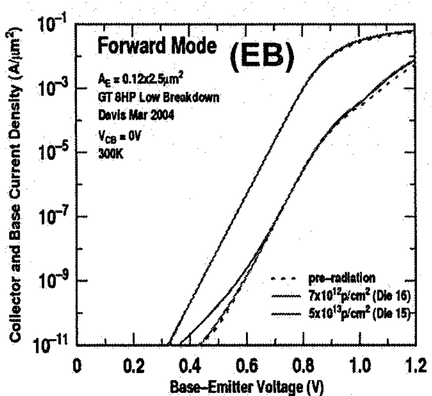
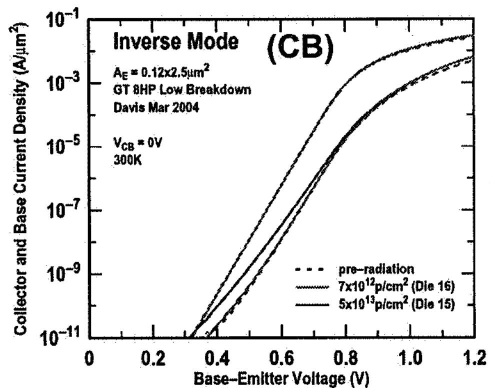
- **Very Minimal Proton Damage in 8HP**
- **Benefit of Epi-base Structure + High Doping Levels**
- **Thus far, VERY encouraging results for TID in SiGe**





63 MeV protons

5HP SEU Data

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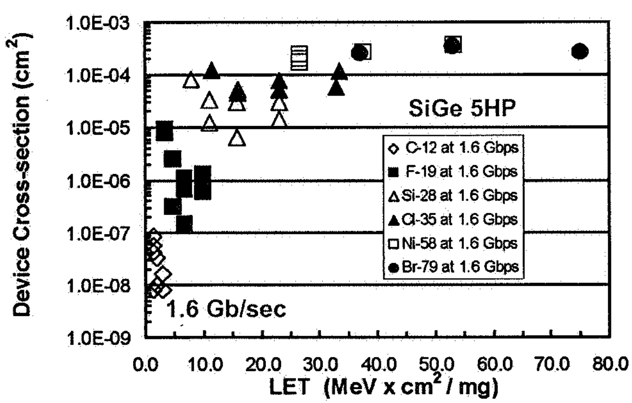
- **Observed SEU Sensitivity in SiGe HBT Shift Registers**
  - low LET threshold + high saturated cross-section (bad news!)
- **III-V Circuit-level Hardening Schemes Not Effective** (CSH)



P. Marshall *et al.*, *IEEE TNS*, 47, p. 2669, 2000.

Circuit-Level RHBD

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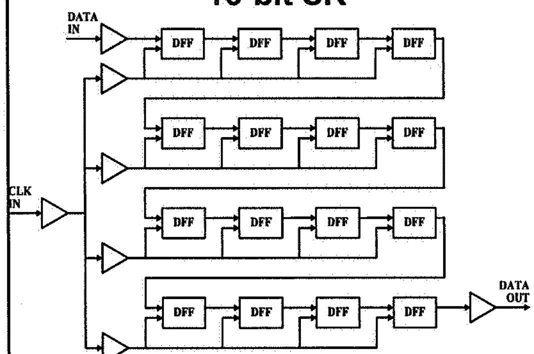
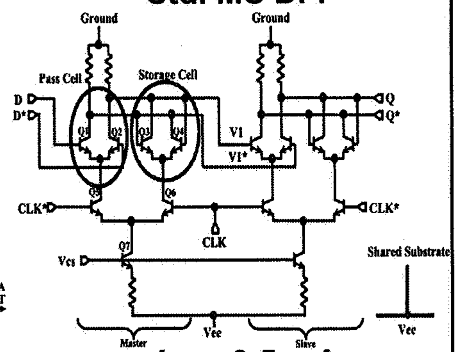
- **16-bit CML shift registers with identical clock-tree arch.**
- **SRs implemented with three types of D-flip flops (DFFs)**
  - –unhardened CML master-slave (MS) DFF (std. SR,baseline)
  - –dual-interleaved MS DFF (DI SR)
  - –gated-feedback cell (GFC) MS DFF (GFC SR)

16-bit SR



Std. MS DFF



I_{tail} = 0.5 mA

Circuit-Level RHBD

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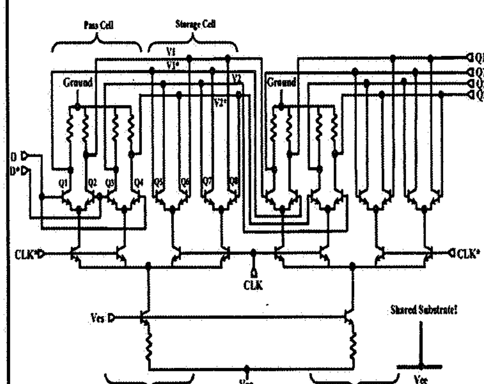
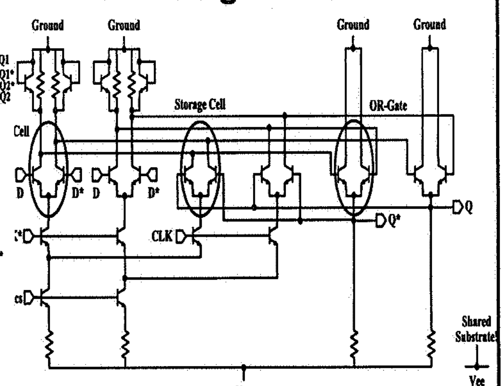
- **DI DFF: limited transistor-level decoupling in storage cell**
- **GFC DFF: OR-gate logic correction and load diode clamps**
- **DI SR and GFC SR featured I_{tail} = 1 mA & std. SR I_{tail} = 0.5 mA**

DI DFF



I_{tail} = 1.0 mA

Master Stage of GFC DFF



I_{tail} = 1.0 mA

Register-Level RHBD

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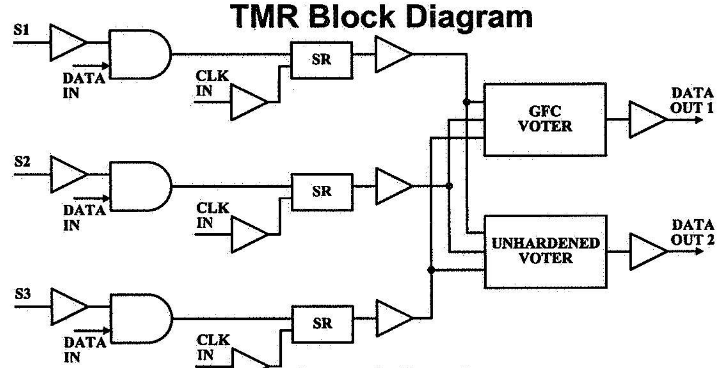
- DI TMR: triple module redundancy in DI SR
- GFC TMR: triple module redundancy in GFC SR
- DI TMR and GFC TMR featured I_{tail} = 0.5 mA
- Voting performed using parallel GFC/unhardened voters

TMR Block Diagram



I_{tail} = 0.5 mA

Device-Level RHBD

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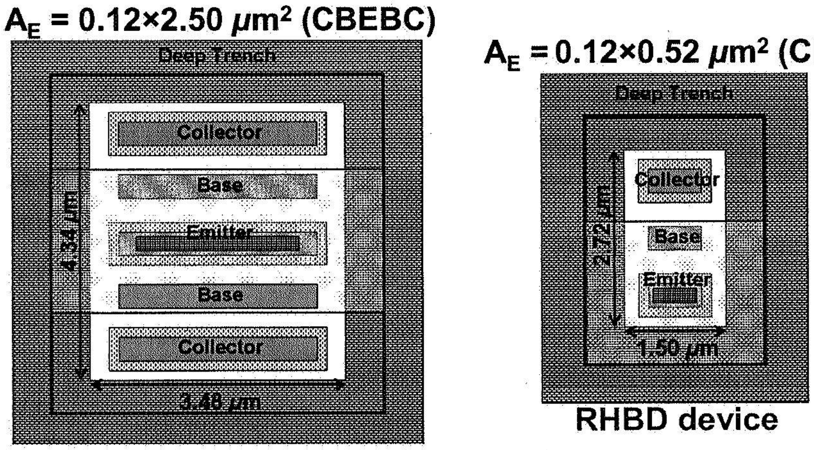
- Reduced deep-trench area ⇒ improved cross-section
- Trench area in CBE (RHBD) device reduced by 73%
- Baseline circuit features CBEBC devices

$A_E = 0.12 \times 2.50\ \mu m^2$ (CBEBC)

$A_E = 0.12 \times 0.52\ \mu m^2$ (CBE)



RHBD device

Experiment

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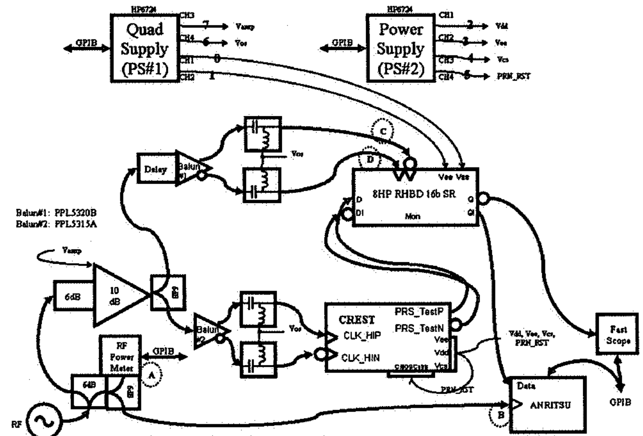
- Heavy ion test was performed at TAMU Cyclotron
- 15 MeV/amu Ne, Ar, Xe ions used at varying incidence
- BERT methods used in testing at data rates ≥50 Mbps



8HP RHBD SR Test Block Diagram

To be presented by Paul W. I

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Cross-Section vs. LET

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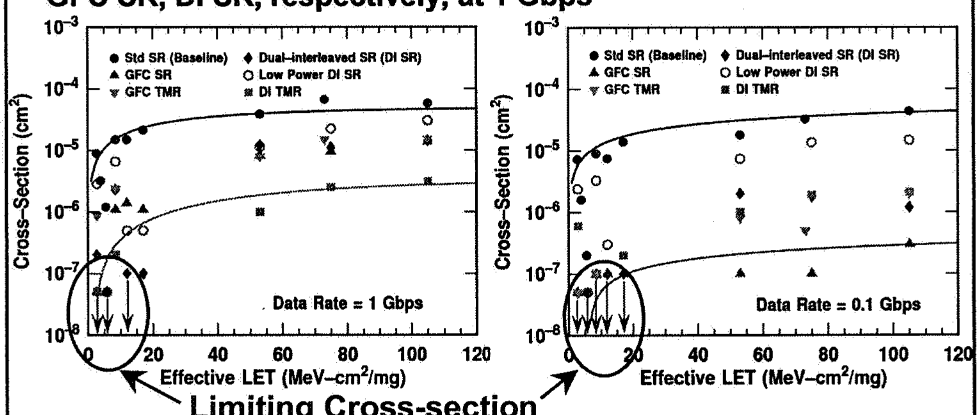
- Std. SR showed the highest σ_{sat} at all data rates
- Low pwr. DI SR with same I_{tail} as std. SR & 2x sensitive nodes, showed 2.5x improvement in σ_{sat} (> expected by 1.85x)
- Limiting σ of 2.8, 5.8, 12 MeV-cm²/mg for DI TMR, GFC SR, DI SR, respectively, at 1 Gbps



To be presented by Paul W. Marshall at the 2006 Single Event Effects Symposium (SEESYM), April 10, 2006 to April 12, 2006 in Long Beach, CA. 12

Cross-Section vs. Speed

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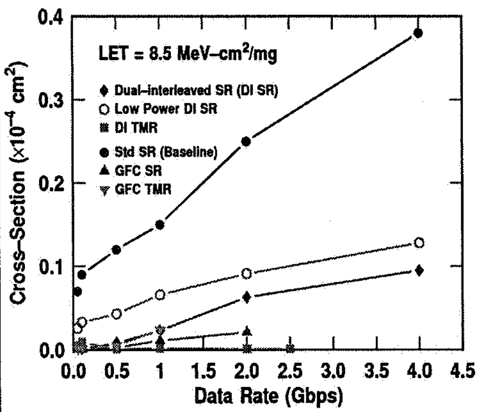
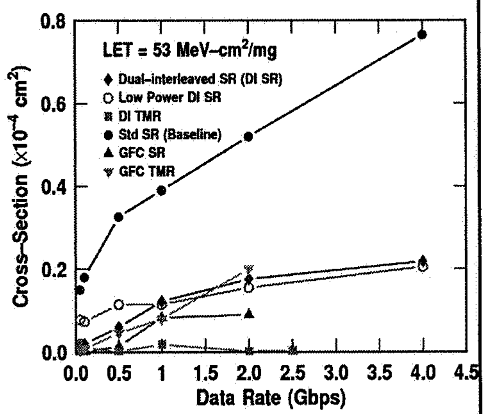
- σ increased with data rate at all LETs except in DI TMR
- While TMR in DI SR improved σ significantly, it offered little improvement in GFC SR and σ degraded with data rate
- No saturation of σ was noted at higher data rates





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Errors / Event vs. Speed

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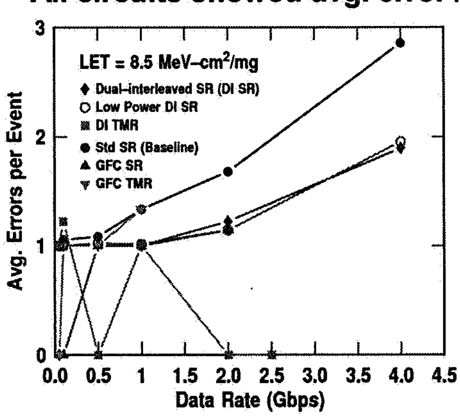
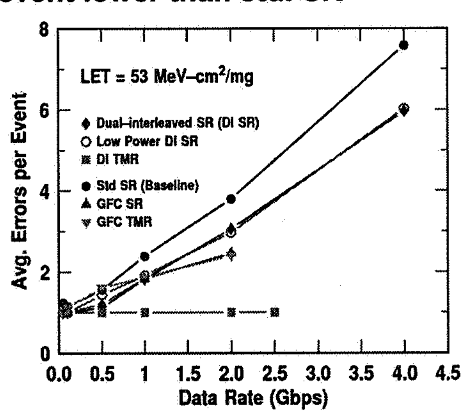
- Avg. errors / event increased linearly with speed at high LETs
- No signature of temporal multiple bit upsets in DI TMR
- Zero avg. error corresponds to limiting σ observed in GFC SR & TMR, and DI SR & TMR
- All circuits showed avg. error / event lower than std. SR





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Comparison

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- LET thresholds were obtained from Weibull fit and $LET_{10\%}$
- L_{th} improvement of 200x observed in DI SR and TMR over std. SR at 1 Gbps

Topology, Power consumption, and estimated Threshold LET for the circuits.

Topology	I_{tail} mA	Overall Power (mW)	Device Type	DFF Area ($\times 10^3\ \mu m^2$)	L_{th} 0.1 Gbps	L_{th} 1 Gbps	$L_{0.1}$ 0.1 Gbps	$L_{0.1}$ 1 Gbps
Std SR	0.5	230	CBEBC	10	0.01	0.01	4.0	1.8
GFC SR	1.0	743	CBE	25	6.00	2.20	10.0	10.0
GFC TMR	0.5	2300	CBE	25	5.00	0.40	11.0	4.6
DI SR	1.0	542	CBE	16	6.00	2.00	10.0	6.2
DI TMR	0.5	1400	CBE	16	0.05	1.70	1.0	9.5
DI SR Low-P	0.5	477	CBE	16	0.05	0.40	1.8	0.4

Summary

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- RHBD techniques were developed for SiGe technology
  - *Circuit-level RHBD techniques:*
    - minimization of local transistor-level cross-coupling
    - triple module redundancy
  - *Device-level RHBD technique:*
    - reduction of DT enclosed sensitive volume
    - utilization of minimum feature-size devices
- Digital building blocks were realized in IBM SiGe 8HP
- Digital blocks were tested for SEU response using heavy-ions
- Low pwr. DI SR showed 2.5x improvement in σ_{sat} over std. SR
- Limiting σ observed for various RHBD enhanced SRs
- TMR in DI SR improved σ significantly
- No temporal multiple bit upsets observed in DI TMR
- Significant improvement in L_{th} observed in RHBD SRs - YEAH!

➔ SEU Hardening Achievable in SiGe using RHBD Techniques!